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10ES33

Third Semester B.E. Degree Examination, June/July 2015
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Express the following Boolean function in canonical min term form :
$F(A,B,C) = \overline{A}\,\overline{B} + C$. **(04 Marks)**

b. Express the following Boolean function in canonical max term form :
$F(A,B,C,D) = \overline{A}B + C\overline{D}$. **(08 Marks)**

c. Simplify the following Boolean function using four variable 'k' map. Realize the simplified expression using NAND gates.
$F(A, B, C, D) = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$. **(08 Marks)**

2 a. Simplify the following Boolean function using Quine – Moclusky's minimization technique.
$F(A, B, C, D) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11, 15)$. **(10 Marks)**

b. Consider the following Boolean equation :
$F(A, B, C, D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$.
Simplify the function F using a 3 variable MEV k – map. Assign the variable D to be the MEV. **(10 Marks)**

3 a. Implement the Boolean functions :
$F_1(x, y, z) = X\overline{Y} + YZ$
$F_2(x, y, z) = \pi m(0,3,5)$
Using a 3 – 8 line decoder IC 74138 with active low outputs. **(08 Marks)**

b. Interface a 10 key keypad to a digital system using a IC 74147 which is a 10 line to BCD priority encoder. Draw the logic diagram and explain the operation with the truth table. **(12 Marks)**

4 a. Implement the Boolean function :
$F(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 7, 8, 9)$
Using a 8 to 1 multiplexer. Draw the logic diagram and explain the operation. Additional gates can be used if required. **(08 Marks)**

b. Explain the operation of a full subtractor with the help of a truth table and Boolean expressions for the outputs. Implement the full subtractor using two numbers of
i) 4 to 1 multiplexers
ii) 2 to 1 multiplexers.
Additional gates if required can be used. **(08 Marks)**

c. Design a one bit binary comparator. **(04 Marks)**

PART – B

5 a. Explain the operation of a gated SR latch with a logic diagram and a truth table. **(06 Marks)**

b. Explain the operation of a positive edge trigged 'D' flip-flop with the help of a logic diagram and truth table. Also draw the relevant waveforms. **(04 Marks)**

c. Draw the output waveforms Q_M and Q_S the outputs of the master and the slave respectively, if the inputs to a master slave JK flip-flop one as indicated below. **(10 Marks)**

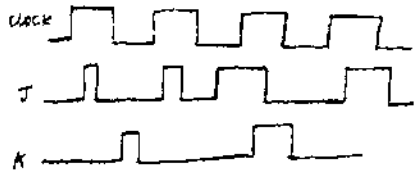

Fig. Q5(c)

6 a. Design a 4 bit binary ripple up counter using negative edge triggered JK flip-flops. Draw the timing diagram with respect to the input cock pulses. Explain the operation. **(10 Marks)**

b. Design a synchronous counter using clocked JK flip-flop for the counting sequence shown below :

Q_2	Q_1	Q_0
0	0	0
0	1	0
0	1	1
1	1	0
1	0	1
0	0	1
0	0	0

(10 Marks)

7 a. Explain mealy and Moore models of a clocked synchronous sequential circuit. **(08 Marks)**

b. Design a synchronous circuit using positive edge triggered JK flip-flops to generate the following sequence :
0 – 1 – 2 – 0 is input x = 0 and
0 – 2 – 1 – 0 is input x = 1
Provide an output which goes high to indicate the non – zero states in the 0 – 1 – 2 – 0 sequence. **(12 Marks)**

8 Construct the excitation table, transition table, state table and state diagram for the sequential circuit shown in Fig. Q8. **(20 Marks)**

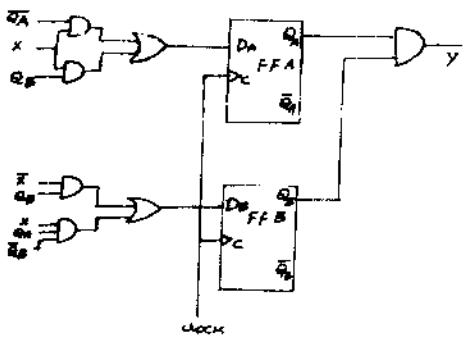

Fig. Q8

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